## DETAILED DESCRIPTION OF THE INVENTION

In the following detailed description of the present invention, a method of applying instructions to a microprocessor in test mode, numerous specific details are set forth in order to provide a thorough understanding of the present invention. However, it will be recognized by one skilled in the art that the present invention may be practiced without these specific details or with equivalents thereof. In other instances, well known methods, procedures, components, and circuits have not been described in detail as not to unnecessarily obscure aspects of the present invention.

## EXEMPLARY TEST ARCHITECTURE

Embodiments of the present invention comprise a test architecture which includes an interface to a test controller located on the same bus as a microprocessor and various registers, memories, etc. under test. The test controller becomes the master during test mode and receives commands and data via the interface and sends data out the interface. The architecture features an instruction queue, which the test controller feeds instructions. Thus, embodiments of the present invention accomplish the functionality of scan logic without the overhead.

Figure 1 illustrates a system in which the present invention may be practiced. The present invention allows an external controller 100 that is external to the circuit under test 150 to issue test commands, data, and addresses over the test interface 110. The data may be exchanged serially in packet data format. The

external controller 100 may be a personal computer or a conventional production tester or the like.

The test controller 120 on the circuit 150 decodes the commands into sequences that exercise the circuit 150. In one embodiment, the commands are in the form of register or memory reads or writes. Thus, the circuit 150 resources appear as some form of R/W memory. The present invention allows the circuit 150 to be tested with the microprocessor running at 100 percent clock speed. Furthermore, structural testing can be performed over the test interface 110. A still further benefit of the present invention is that all input/output pins may be structurally tested without probing them. However, Current output high/low and Voltage output high/low type measurements may require probing.

The test interface 110 (e.g., the integrated circuit pins) is not dedicated to testing the circuit 150 and hence is used for another function when not in test mode. For example, it may be used to output the signal from a crystal oscillator within the circuit 150. The commands and data are received serially, in the preferred embodiment. Test interface 110 may be a two pin interface, in this embodiment. One pin may be a bi-directional data pin. The other pin may be used for a clock, which may be user supplied to clock in the data, in one embodiment. However, the present invention is well suited to a test interface 110 with any number of pins. Furthermore, the circuit 150 under test may have any number of pins. When the circuit 150 has relatively few pins (e.g., four) it may become more important to be able to use the test pins for dual purposes. However, even if many pins are available, the present invention may still provide

more efficient use of resources and allow a circuit 150 to have more functionality by re-using pins.

Figure 2 shows a diagram of circuit 150 in accordance with one embodiment of the present invention. As depicted in Figure 2, the on-chip test controller 120 is coupled to the test interface 110. The circuit 150 also comprises a microprocessor 210, which executes instructions fed in from the multiplexer 270. When the test controller 120 desires control of the bus 201 it sends a bus master request to the microprocessor 210, which returns a bus master grant, as is well understood in the art.

The test controller 120 controls the multiplexer 270. However, it is also possible to allow the microprocessor 210 to have control over the multiplexer 270, as well. In this embodiment, the microprocessor 210 reacts to the instruction it is executing by sending a signal to the multiplexer 270, which causes the multplexer 270 to feed the microprocessor 210 commands from a different source.

The test controller 120 receives commands from the external interface 110 and transfers them via the system bus 201 to the instruction queue 240. The Supervisory Read Only Memory (SROM) 250 contains instructions which are to be run in the microprocessor 210 while under test mode. Thus, the present invention is able force the microprocessor 210 to execute a set of pre-determined instructions. When such instructions are executed the circuit 150 may be in what is referred to in this application as a supervisory state, which is part of the test mode. In a preferred embodiment, during test mode only instructions from the